Semiconductor Layout Design Protection Guide (India)

Protecting IC layout designs under the Semiconductor Integrated Circuits Layout-Design Act 2000

HOW TO USE THIS TEMPLATE	
1.	This document: Semiconductor Layout Design Protection Guide (India).
2.	Fill all bracketed fields before use.
3.	Template only — not a substitute for qualified legal advice.

1. LEGAL FRAMEWORK AND SCOPE

The SICLD Act 2000. The Semiconductor Integrated Circuits Layout-Design Act 2000 provides sui generis protection for integrated circuit layout designs — the three-dimensional disposition of circuit elements and interconnections in a semiconductor chip. Enacted under TRIPS Agreement Article 35.

What Is Protected. A layout design: three-dimensional disposition of elements of an integrated circuit and their interconnections, where at least one element is active. Must be: original (result of creator's own effort; not commonplace among creators); and not commonplace in the semiconductor industry at the time of creation.

Who Should Register. Chip design companies; VLSI startups; IoT hardware companies designing custom SoCs or ASICs; electronics product companies with proprietary circuit designs; fabless semiconductor companies; and university spin-outs commercialising chip designs.

Term of Protection. 10 years from the earlier of: (a) the filing date; or (b) the first date of commercial exploitation in any WTO member country. No renewal — protection ends after 10 years.

2. REGISTRATION PROCESS

Filing. File Form SICLD-1 at the Semiconductor Integrated Circuits Layout-Design Registry under MeitY. Documents: completed application form; copy of the layout design (drawings or electronic format); photographs if available; declaration of originality; details of first commercial exploitation; and identity and address proof. Fee: Rs. 20,000 (one-time flat fee — no annual renewals).

Confidentiality Option. The SICLD Act allows applicants to request that portions of the filed layout design be kept confidential to protect trade secrets. Specify this request in the application — it allows IP protection without full public disclosure of proprietary design details.

Rights Granted. Exclusive rights to: reproduce the layout design; import, sell, or distribute the layout design; and import, sell, or distribute an integrated circuit incorporating the protected layout design. Criminal penalties for infringement: imprisonment up to 3 years and fine up to Rs. 10 lakhs.

3. STRATEGIC CONSIDERATIONS

SICLD + Patent Combination. Most valuable chip innovations can be protected under both SICLD (for the layout topology) and patents (for the novel functional aspects). SICLD protects the specific topological realisation; patents protect the inventive method regardless of topological implementation. File both simultaneously for maximum protection.

SICLD vs Copyright. Circuit diagrams and schematic drawings may also be protected as artistic works under the Copyright Act 1957 — separately from SICLD. SICLD protects the three-dimensional layout; copyright protects two-dimensional schematic representations and technical documentation. Use both.

Open Hardware Strategy. Some chip startups release layout designs under open hardware licences (CERN OHL, TAPR OHL). This is irreversible — once released under an open licence, SICLD protection cannot be obtained. Make this decision deliberately with full commercial consideration.

International Protection. India is a TRIPS member, which requires all WTO members to protect IC layout designs. For chips manufactured in Taiwan, China, or South Korea, engage local IP counsel in each manufacturing and market jurisdiction.

4. ENFORCEMENT AND LICENSING

Detecting Infringement. SICLD infringement typically occurs through: reverse engineering (taking apart a chip and reconstructing the layout); copying of GDSII or other layout files; or using a layout design in a different chip product. Detection methods: comparing chip dies under electron microscopy; comparing technical performance characteristics; finding evidence of design file theft through cybersecurity investigation.

Licensing SICLD Designs. Layout designs can be licensed separately or bundled with patent licences. Key licensing terms: specific layout version; permitted process nodes and foundries; field of use restrictions; royalty basis (per chip, per wafer, or percentage of revenue); and improvement rights.

Enforcement Action. Civil suit in the High Court: injunction; damages; delivery up. Criminal complaint under the SICLD Act: imprisonment up to 3 years and fine up to Rs. 10 lakhs. The criminal sanction is a meaningful deterrent in the semiconductor industry.

IMPORTANT NOTE

Working template for Semiconductor Layout Design Protection Guide (India). Verify requirements with a qualified IP advocate.

CHIP DESIGN IP STRATEGY FOR INDIAN SEMICONDUCTOR STARTUPS

India's semiconductor industry is experiencing significant policy-driven growth through the India Semiconductor Mission (ISM), Semicon India Programme, and Production Linked Incentive (PLI) schemes. For semiconductor startups navigating this landscape, building a strong IP foundation is both commercially essential and a prerequisite for accessing government support. India Semiconductor Mission IP

implications: the ISM requires applicants to demonstrate IP ownership and provide IP protection plans for the technology being funded. A startup applying for ISM support should have: design registrations for key layout topologies; patent filings for novel circuit architectures or design methodologies; and clear IP ownership documentation (all founder assignments, employee IP agreements, and contra

ctor assignments in place). The VLSI IP ecosystem: India has a growing ecosystem of VLSI design service companies, EDA tool providers, and IP core vendors. For startups licensing third-party IP cores (processor cores, memory controllers, PHY IP): verify the licence covers all intended use cases (ASIC design, prototype, full production); confirm the licence includes the right to have the chip manuf

actured at the chosen foundry; assess what happens to your chip design if the IP core vendor is acquired or goes out of business (software escrow for critical IP cores); and understand the royalty model (per-chip royalty vs upfront lump sum). Process node IP considerations: different foundry process nodes come with different design rules, standard cell libraries, and associated IP. The standard ce

ll libraries and PDKs (Process Design Kits) provided by foundries are licensed, not owned — confirm your licence allows you to build a commercial product and ship it globally. Some foundry licences have field-of-use restrictions or export compliance requirements. TSMC, Samsung, GLOBALFOUNDRIES, and Indian foundries (ISMC, SCL Chandigarh) each have different licence terms — review carefully with yo

ur IP attorney before committing to a process node.

ADDITIONAL COMPLIANCE GUIDANCE AND BEST PRACTICES

ADDITIONAL GUIDANCE ON COMPLIANCE AND BEST PRACTICES. Indian IP law continues to evolve rapidly, with the Patent Office, Trade Marks Registry, and Copyright Office all implementing digital transformation initiatives that affect how IP is filed, prosecuted, and enforced. The Patents Amendment Rules 2024 introduced new provisions for startup fee concessions and updated the examination procedure timelines. The Trade Marks Act 1999 has been interpreted by courts in a growing body of decisions that clarify how confusion is assessed, how well-known

marks are recognised, and how bad faith is established. The DPDP Act 2023 has implications for IP-linked customer data and product development processes. For each IP action described in this document, the Company should consult a qualified IP advocate licensed to practice before the Indian Patent Office and Trade Marks Registry. IP advocates combine technical expertise with legal training specific to Indian IP law. When selecting an IP advocate, assess: their specific experience in your technology sector or product category;

their track record at the relevant Patent Office branch or Trade Marks Registry; and their ability to coordinate international filings through their network of foreign associates. The IP Manager should maintain a master calendar tracking all IP filing deadlines, prosecution response deadlines, renewal dates, and opposition window close dates. IP deadlines are typically non-extendable and missing them can result in permanent loss of rights. Use a dedicated IP management tool or a carefully maintained calendar system with triple-reminder alerts. Document

all IP decisions and the reasoning behind them. When the Company decides not to file a patent application for a particular technology, document the decision and reasoning. When a trademark opposition is decided not to pursue, document the decision. This decision trail is important for investor due diligence, management continuity, and defence of subsequent IP disputes. Build a quarterly IP Committee meeting cadence: the IP Manager, CTO or Head of Product, CFO, and CEO should review IP programme status, upcoming

decisions, and strategic IP priorities every quarter. This keeps IP on the leadership agenda and ensures that commercial and technical strategy is aligned with IP investment decisions. The IP Committee meeting should produce a brief written record of decisions taken and actions assigned. International IP coordination requires proactive management of priority deadlines. The Paris Convention priority period of 12 months for patents and 6 months for trademarks and designs starts from the Indian filing date. If international protection is planned,

calendar these priority deadlines immediately on the Indian filing date. The cost of filing internationally increases significantly if priority is not claimed because prior art in the intervening period may destroy novelty. Budget for professional indemnity insurance for the IP function. As IP becomes a larger component of the Company's value and IP decisions involve significant financial stakes, the IP Manager and the Company's IP counsel should be appropriately insured against errors and omissions. Review the IP programme's documentation quality

annually. The best IP strategy is undermined by poor documentation. Every IP right should have a complete file: the registration or application document, all prosecution history, all renewal receipts, and all related agreements. Files should be backed up in at least two locations and access-controlled to prevent inadvertent deletion. Template only. Not legal advice. Consult a qualified IP advocate for all decisions affecting the Company's intellectual property rights.